Amendments to the Specification:

Please replace paragraph 0036, with the following amended paragraph:

With the frontside substrate installed, the semiconductor wafer is supported for backside thinning. As mentioned, the wafer substrate layer 12 is initially provided with the normal or conventional thickness need for self support of the wafer. As such, the wafer layer 12 is too thick for many desirable examination techniques to be performed for backside analysis of the whole wafer. Accordingly, the thickness of wafer layer 12 is reduced preferably using a conventional technique, such as, for example, ion-beam milling techniques such as those described in United States Patent No. 5,786,236; backside reactive ion etches disclosed in United States Patent No. 6,294,395; milling or ion beam etching techniques, such as those disclosed in United States Patent Nos. 5,698,474 and 6,281,025; oxidation techniques, such as those described in United States Patent No. 4,615,762; and/or chemical mechanical polishing (CMP) techniques such as those employed in United States Patent No. 5,162,251.

Please replace paragraph 0038, with the following amended paragraph:

Accordingly, it is generally preferred that the thickness of wafer substrate 12 be reduced using precision surfacing processing machines such as the precision in-feed wafer grinder and whole wafer surface finishing tools mentioned above.